

Last DSM Algorithm
2008 Version E – PP Running

14th February 2008

Input Bits

NOTE: Only those bits that are used in this algorithm are listed here.

Input Channel	Bit Description
0	CTB Information Unused
1	VTX Information Bit 0 – BBC TAC difference in window Bits 1:15 – Unused
2	CTB Topology, VPD and MTD Information Bit 0 – VPD TAC difference in window-0 Bit 1:5 – Unused Bit 6 – MTD trigger Bit 7:15 – Unused
3	EMC Information Bits 0:1 – Barrel JP bits Bits 2:3 – Barrel HT bits (thresholds #0, #1 and #2 coded into 2 bits) Bits 4:5 – Unused Bit 6 – Barrel HT.TP bit Bits 7:8 – Endcap JP bits Bits 9:11 Unused Bit 12 – Endcap HT.TP bit Bits 13:14 – Unused Bit 15 – Barrel+Endcap Total Energy bit
4	RAT Board Bits 0 - TOF Bits 1:10 – Unused Bit 11 – FMS LED Bits 12:15 - Unused
5	FPD Information Bit 0 – Unused Bit 1 – FMS HT threshold-1 Bits 2:4 – Unused Bit 5 – Any FPD-East module > threshold-1 Bit 6 – Any FPD-East module > threshold-2 Bit 7 – Both FPD-East modules > threshold-0 AND sum > threshold-3 Bits 8:15 - Unused
6	Special Trigger Requests Bits 0:13 - Unused Bit 14 – Zero-bias bit Bit 15 - Unused
7	Unused

Registers

Register	Register Description
0	Pre-scale for BBC logic
1	Pre-scale for FMS logic

Output Bits

Bit	Description
Bits 0:15	
0	MTD
1	TOF
2	Pre-scaled FMS
3	FMS
4	FPDE or FMS-LED
5	BEMC+EEMC ETOT
6:7	BEMC HT bits (coding three thresholds)
8	EEMC JP0
9	BEMC JP0 or EEMC JP1
10	BEMC JP1 or EEMC JP2
11	BEMC or EEMC HTTP
12	VPD
13	BBC
14	Pre-scaled BBC
15	Zero bias
Bits 16:31	Same definitions as bits 0:15

Internal Logic

- The MTD input bit received on channel 2 is passed through to the output unmodified
- The TOF input bit received on channel 4 is passed through to the output unmodified
- The FMS bit received on channel 5 (at least 1 FMS HT > threshold-1) is passed through to the output unmodified.
- The FMS bit is also pre-scaled using the 8-bit value specified in register 1. The output bit is set when the pre-scale counter reaches 1, at which point the counter is reset to the starting value specified in register 1.
- $FPDE = (Any\ FPD-East\ module > threshold-2) \text{ or } (Both\ FPD-East\ modules > threshold-0 \text{ AND } sum > threshold-3)$
The result is OR'ed with the FMS LED bit to make output bit 4
- The BEMC+EEMC total energy bit received on channel 3 is passed through to the output unmodified.
- The BEMC high tower packed input bits received on channel 3 are passed through to the output unmodified (thresholds 0, 1 and 2 packed into a 2-bit integer)

- The BEMC and EEMC jet patch (JP) bits received on channel 3 are unpacked. The bits are then OR'ed together to produce output bits 8, 9 and 10.
- The BEMC and EEMC HT.TP bits received on channel 3 are OR'ed together to make output bit 11.
- The VPD bit is a copy of the bit labeled "VPD TAC difference in window 0" received from CB201 on Input Channel 2. It is formed from the difference between the TAC values of the fastest GOOD hits on each side (East and West). A "good" hit is defined as one in which the ADC value was over threshold and its associated TAC value was inside a window. Since the VPD TAC difference bit has not been combined with any of the VPD ADC sum threshold bits the logic can be satisfied if there is exactly one good hit on each side of the VPD.
- The BBC bit is a copy of the bit labeled "BBC TAC difference in window" received from VT201 on Channel 1. It is formed in the same way as the VPD bit.
- The BBC bit is also pre-scaled using the 8-bit value specified in register 0. The output bit is set when the pre-scale counter reaches 1, at which point the counter is reset to the starting value specified in register 0.
- The zero-bias input bit received on channel 6 is passed through to the output unmodified.