TCU-4 Memory Map
December 16, 2014
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Overview

Memory Block	*Starting Address*	*Ending Address*	*Number of Addresses*
Mother CSRs	0x YY00 0000	0x YY3f fffc	2^{20} (1 M)
Daughter CSRs	0x YY40 0000	0x YY7f fffc	
General Registers	0x YY40 0000	0x YY4f fffc	2^{18} (256K)
Trigger Registers	0x YY50 0000	0x YY5f fffc	2^{18} (256K)
Output Registers	0xYY60 0000	0x YY6f fffc	2^{18} (256K)
Counter Registers	0xYY70 0000	0x YY7f fffc	2^{18} (256K)
Daughter Memory	0x YY80 0000	0x YYff fffc	
DSM Input Memory	0x YY80 0000	0x YY8f fffc	2^{18} (256K)
Busy Input Memory	0x YY90 0000	0x YY93 fffc	2^{16} (64K)
Flash Memory Registers	0x YYa0 0000	0x YYa0 0004	2
Flash Memory	0x YYb0 0000	0x YYb3 fffc	2^{16} (64K)

Mother CSRs

ID: Name	*Address*	*Functionality (default)*	*Access*
0:Mother firmware revision	0x YY00 0000	0xABCDmmmm	R
1:RHIC Clock and Control Status	0x YY00 0004	D0: RCC_halt D1: RCC_latch D2: RCC_run_stop (these default to '1' when unconnected)	R
2:Mother firmware date	0x YY00 0008	0xDAyymmdd – Date of this revision	R
3:RCC/Local clock mode	0x YY00 000c	D0: 0=RCC, 1=Local	RW
4:Local mode run/stop	0x YY00 0010	D0: 0=Stop, 1=Run	RW
5:Operation Control	0x YY00 0014	D0: 0=Load, 1=Armed	RW
	0x YY00 0018 – 0x YY3f fffc	Space available for extra registers	

Daughter CSRs

General Registers

ID: Name	*Address*	*Functionality (default)*	*Access*
0: Daughter firmware revision	0x YY40 0000	0xDCBAmmnn (Major and Minor revision)	R
1: Daughter firmware date	0x YY40 0004	0xDAyymmdd – Date of this revision	R
2: DSM Cables Connected	0x YY40 0008	D(7,0)	R
3: Read/writable test register	0x YY40 000c		RW
4: TCD clock source	0x YY40 0010	D0: 0=TCUI, 1=TCU	RW
5-7: Reserved	0x YY40 0014 – 0x YY40 001c	Reserved for future use	
8: 8xRHIC Clock Control	0x YY40 0020	D0: Reset 8xRHIC clock D1: Reset 8xRHIC strobes	W
9: 8xRHIC Clock Status	0x YY40 0024	D0:1 = PLL Locked on RHIC clock 0 = PLL Not locked D1: Input RHIC clock stopped D2: PLL Feedback stopped	R
	0x YY40 0028 – 0x YY4f fffc	Space available for extra registers	

Trigger Registers

General Trigger Registers

0: Contamination Condition 1, on	0x YY50 0000	D(31,0): DSM bits (31,0)	RW
1: Contamination Condition 1, on	0x YY50 0004	D(31,0): DSM bits (63,32)	RW
2: Contamination Condition 1, on	0x YY50 0008	D(31,0): DSM bits (95,64)	RW
3: Contamination Condition 1, on	0x YY50 000c	D(31,0): DSM bits (127,96)	RW
4: Contamination Condition 1, off	0x YY50 0010	D(31,0): DSM bits (31,0)	RW
5: Contamination Condition 1, off	0x YY50 0014	D(31,0): DSM bits (63,32)	RW
6: Contamination Condition 1, off	0x YY50 0018	D(31,0): DSM bits (95,64)	RW
7: Contamination Condition 1, off	0x YY50 001c	D(31,0): DSM bits (127,96)	RW
8: Contamination Length	0x YY50 0020	D(31,0): in RS units	RW
9: Internal Busy Enable	0x YY50 0024	D(15,0): Enable per detector	R/W
10: Internal Busy Length	0x YY50 0028	D(31,0): in RS units	R/W
11: Contamination and Busy Reset	0x YY50 002c	D0: Reset contamination counter D1: Reset internal busy counters	W
12: Contamination and Busy Status	0x YY50 0030	D(15,0): Current status of internal busy bits 1 = Busy 0 = Live D(16): Current status of contamination bit 1 = Contamination present 0 = No contamination	R
13: Contamination Enable/Disable	0x YY50 0034	D0: 0=Disable, 1=Enable D1: Condition 1 Disable(0)/Enable(1) D2: Condition 2 Disable(0)/Enable(1) D3: Condition 3 Disable(0)/Enable(1) D4: Condition 4 Disable(0)/Enable(1)	R/W
14-15: Reserved	0x YY50 0038 – 0x YY50 003c	Space available for extra registers	
16: Contamination Condition 2, on	0x YY50 0040	D(31,0): DSM bits (31,0)	RW
17: Contamination Condition 2, on	0x YY50 0044	D(31,0): DSM bits (63,32)	RW
18: Contamination Condition 2, on	0x YY50 0048	D(31,0): DSM bits (95,64)	RW
19: Contamination Condition 2, on	0x YY50 004c	D(31,0): DSM bits (127,96)	RW
20: Contamination Condition 2, off	0x YY50 0050	D(31,0): DSM bits (31,0)	RW
21: Contamination Condition 2, off	0x YY50 0054	D(31,0): DSM bits (63,32)	RW
22: Contamination Condition 2, off	0x YY50 0058	D(31,0): DSM bits (95,64)	RW
23: Contamination Condition 2, off	0x YY50 005c	D(31,0): DSM bits (127,96)	RW
24: Contamination Condition 3, on	0x YY50 0060	D(31,0): DSM bits (31,0)	RW
25: Contamination Condition 3, on	0x YY50 0064	D(31,0): DSM bits (63,32)	RW
26: Contamination Condition 3, on	0x YY50 0068	D(31,0): DSM bits (95,64)	RW
27: Contamination Condition 3, on	0x YY50 006c	D(31,0): DSM bits (127,96)	RW
28: Contamination Condition 3, off	0x YY50 0070	D(31,0): DSM bits (31,0)	RW
29: Contamination Condition 3, off	0x YY50 0074	D(31,0): DSM bits (63,32)	RW
30: Contamination Condition 3, off	0x YY50 0078	D(31,0): DSM bits (95,64)	RW
31: Contamination Condition 3, off	0x YY50 007c	D(31,0): DSM bits (127,96)	RW
32: Contamination Condition 4, on	0x YY50 0080	D(31,0): DSM bits (31,0)	RW
33: Contamination Condition 4, on	0x YY50 0084	D(31,0): DSM bits (63,32)	RW
34: Contamination Condition 4, on	0x YY50 0088	D(31,0): DSM bits (95,64)	RW
35: Contamination Condition 4, on	0x YY50 008c	D(31,0): DSM bits (127,96)	RW
36: Contamination Condition 4, off	0x YY50 0090	D(31,0): DSM bits (31,0)	RW
37: Contamination Condition 4, off	0x YY50 0094	D(31,0): DSM bits (63,32)	RW
38: Contamination Condition 4, off	0x YY50 0098	D(31,0): DSM bits (95,64)	RW
39: Contamination Condition 4, off	0x YY50 009c	D(31,0): DSM bits (127,96)	RW

	0x YY50 00a0 – 0x YY50 fffc	Space available for extra registers	

Specific Trigger Registers
(for trigger xx = 0:63)

ID: Name	*Address*	*Functionality*	*Access*
0: Condition 1, on	0x YY51 xx00	D(31,0): DSM bits (31,0)	RW
1: Condition 1, on	0x YY51 xx04	D(31,0): DSM bits (63,32)	RW
2: Condition 1, on	0x YY51 xx08	D(31,0): DSM bits (95,64)	RW
3: Condition 1, on	0x YY51 xx0c	D(31,0): DSM bits (127,96)	RW
4: Condition 1, off	0x YY51 xx10	D(31,0): DSM bits (31,0)	RW
5: Condition 1, off	0x YY51 xx14	D(31,0): DSM bits (63,32)	RW
6: Condition 1, off	0x YY51 xx18	D(31,0): DSM bits (95,64)	RW
7: Condition 1, off	0x YY51 xx1c	D(31,0): DSM bits (127,96)	RW
NOTE: Registers 8:31 for Conditions 2:4 are only implemented for triggers xx=0:7. The other triggers (xx=8:63) have just a single condition so these registers are ignored.			
8: Condition 2, on	0x YY51 xx20	D(31,0): DSM bits (31,0)	RW
9: Condition 2, on	0x YY51 xx24	D(31,0): DSM bits (63,32)	RW
10: Condition 2, on	0x YY51 xx28	D(31,0): DSM bits (95,64)	RW
11: Condition 2, on	0x YY51 xx2c	D(31,0): DSM bits (127,96)	RW
12: Condition 2, off	0x YY51 xx30	D(31,0): DSM bits (31,0)	RW
13: Condition 2, off	0x YY51 xx34	D(31,0): DSM bits (63,32)	RW
14: Condition 2, off	0x YY51 xx38	D(31,0): DSM bits (95,64)	RW
15: Condition 2, off	0x YY51 xx3c	D(31,0): DSM bits (127,96)	RW
16: Condition 3, on	0x YY51 xx40	D(31,0): DSM bits (31,0)	RW
17: Condition 3, on	0x YY51 xx44	D(31,0): DSM bits (63,32)	RW
18: Condition 3, on	0x YY51 xx48	D(31,0): DSM bits (95,64)	RW
19: Condition 3, on	0x YY51 xx4c	D(31,0): DSM bits (127,96)	RW
20: Condition 3, off	0x YY51 xx50	D(31,0): DSM bits (31,0)	RW
21: Condition 3, off	0x YY51 xx54	D(31,0): DSM bits (63,32)	RW
22: Condition 3, off	0x YY51 xx58	D(31,0): DSM bits (95,64)	RW
23: Condition 3, off	0x YY51 xx5c	D(31,0): DSM bits (127,96)	RW
24: Condition 4, on	0x YY51 xx60	D(31,0): DSM bits (31,0)	RW
25: Condition 4, on	0x YY51 xx64	D(31,0): DSM bits (63,32)	RW
26: Condition 4, on	0x YY51 xx68	D(31,0): DSM bits (95,64)	RW
27: Condition 4, on	0x YY51 xx6c	D(31,0): DSM bits (127,96)	RW
28: Condition 4, off	0x YY51 xx70	D(31,0): DSM bits (31,0)	RW
29: Condition 4, off	0x YY51 xx74	D(31,0): DSM bits (63,32)	RW
30: Condition 4, off	0x YY51 xx78	D(31,0): DSM bits (95,64)	RW
31: Condition 4, off	0x YY51 xx7c	D(31,0): DSM bits (127,96)	RW
32: Detector on	0x YY51 xx80	D(15,0)	RW
33: Detector off	0x YY51 xx84	D(15,0)	RW
34: Trigger Enable/Disable	0x YY51 xx88	D0: 0=Disable, 1=Enable NOTE: Bits D1:D4 are only implemented for triggers xx=0:7, i.e. the triggers with multiple conditions. The other triggers (xx=8:63) have just a single condition which is always enabled so these bits are ignored. D1: Condition 1 Disable(0)/Enable(1) D2: Condition 2 Disable(0)/Enable(1) D3: Condition 3 Disable(0)/Enable(1) D4: Condition 4 Disable(0)/Enable(1)	RW
35: Contamination Enable/Disable	0x YY51 xx8c	D0: 0=Ignore, 1=Use contamination bit	RW

36: Prescale	0x YY51 xx90	D(31,0)	RW
37: Prescale Counter Start	0x YY51 xx94	D(31,0)	RW
38: Prescale Fraction	0x YY51 xx98	D(6,0)	RW
39: Prescale Fraction Start	0x YY51 xx9c	D(6,0)	RW
40: Action Word	0x YY51 xxa0	D(15,0): AW Detector Bitmask D(19,16): AW DAQ Command D(23,20): AW TRG Command D(27,24): AW DAQ10k Bitmask	R/W
41: Conditional Detectors	0x YY51 xxa4	D(15,0): Conditional Detector Bitmask	R/W
	0x YY51 xxa8 – 0x YY51 xxfc	Space available for extra registers for this trigger	
	0x YY51 4000 – 0x YY5f fffc	Space available for extra registers	

Output Registers

0: Local Address Control	0x YY60 0000	D0: Reset to zero D1: Copy current value to CSR16 D2: Increment by one	W
1: Read Local Address	0x YY60 0004	D(31,0): Address counter value	R
2: Output Data Delay	0x YY60 0008	D(4,0): Number of 8xRHIC clock ticks of output delay (values of 0 – 17 are valid)	RW
3: Force Trigger AW	0x YY60 000c	D(15,0): AW Det Bitmask D(19,16): AW DAQ Command D(23,20): AW TRG Command	W
4: FIFO Reset	0x YY60 0010	D0: Clear Token FIFO D1: Clear Response FIFOs D2: Clear Info FIFOs	W
5: Self-Trigger Enable/Disable	0x YY60 0014	D0: 0=Disable, 1=Enable	R/W
6-7: Reserved	0x YY60 0018 – 0x YY60 001c	Space available for extra output control registers.	
8: FIFO Status	0x YY60 0020	D0: Token FIFO Empty D1: Token FIFO Full D2: Response FIFO Empty D3: Response FIFO Full D4: Info FIFO 1 Empty D5: Info FIFO 1 Full D6: Info FIFO 2 Empty D7: Info FIFO 2 Full D8: Info FIFO 3 Empty D9: Info FIFO 3 Full D10: Info FIFO 4 Empty D11: Info FIFO 4 Full D12: Info FIFO 5 Empty D13: Info FIFO 5 Full D14: Info FIFO 6 Empty D15: Info FIFO 6 Full D16: Info FIFO 7 Empty D17: Info FIFO 7 Full D18: Info FIFO 8 Empty D19: Info FIFO 8 Full D20: Info FIFO 9 Empty D21: Info FIFO 9 Full D22: Info FIFO 10 Empty D23: Info FIFO 10 Full	R

9-15: Reserved	0x YY60 0024 – 0x YY60 003c	Space available for extra FIFO status registers	
16: Token FIFO	0x YY60 0040	D(11,0): Token	W
17: Response FIFO 1	0x YY60 0044	D(23,0): Action Word	W
18: Response FIFO 2	0x YY60 0048	D(11,0): Token	W
19: Info FIFO 1	0x YY60 004c	D(15,0): AW Det Bitmask D(19,16): AW DAQ Command D(23,20): AW TRG Command D(27,24): AW DAQ10k Command D(28): Contamination bit D(31,29): Trigger type bitmask 001 = new trigger 010 = response 100 = forced trigger	R
20: Info FIFO 2	0x YY60 0050	D(11,0): Token	R
21: Info FIFO 3	0x YY60 0054	D(31,0): DSM tree bits (31,0)	R
22: Info FIFO 4	0x YY60 0058	D(31,0): DSM tree bits (63,32)	R
23: Info FIFO 5	0x YY60 005c	D(31,0): DSM tree bits (95,64)	R
24: Info FIFO 6	0x YY60 0060	D(31,0): DSM tree bits (127,96)	R
25: Info FIFO 7	0x YY60 0064	D(31,0): Active triggers (31,0)	R
26: Info FIFO 8	0x YY60 0068	D(31,0): Active triggers (63,32)	R
27: Info FIFO 9	0x YY60 006c	D(15,0): External Detector Status 1 = Live 0 = Busy D(32,16): Internal Detector Status 1 = Busy 0 = Live NOTE: External and Internal signals have opposite polarities.	R
28: Info FIFO 10	0x YY60 0070	D(31,0): DSM address	R
	0x YY60 0074 – 0x YY60 fffc	Space available for more Info FIFOs	

Counter Registers

General Counter Registers

0: Counter Control	0x YY70 0000	D0: Clear all counters D1: Latch counter values D2: Done reading	W
1: Counter Status	0x YY70 0004	D0: Data ready D1: Error D2: Overflow	R
	0x YY70 0008 – 0x YY70 001c	Reserved for future control and status registers	

Specific Counter Registers

0: Bunch Crossing (lo)	0x YY70 0020	D(0-31): Counter data 32 LSB	R
1: Bunch Crossing (hi)	0x YY70 0024	D(0-7): Counter data 8 MSB	R
2: TCU dead (lo)	0x YY70 0028	D(0-31): Counter data 32 LSB	R
3: TCU dead (hi)	0x YY70 002c	D(0-7): Counter data 8 MSB	R
4: Triggers (lo)	0x YY70 0030	D(0-31): Counter data 32 LSB	R
5: Triggers (hi)	0x YY70 0034	D(0-7): Counter data 8 MSB	R

6: Responses (lo)	0x YY70 0038	D(0-31): Counter data 32 LSB	R
7: Responses (hi)	0x YY70 003c	D(0-7): Counter data 8 MSB	R
	0x YY70 0040 – 0x YY70 fffc	Available space for extra registers	
For each Detector ZZ: ZZ is in the range 0 to 15 For each ZZ there is a pair of registers Register Address = 0xYY710000 + (ZZ<<3) + offset			
ZZ-0: Det-Live-ZZ (lo)	Offset = 0x0	D(0-31): Counter data 32 LSB	R
ZZ-1: Det-Live-ZZ (hi)	Offset = 0x4	D(0-7): Counter data 8 MSB	R
So, for example…			
ZZ=0			
0-0: Det-Live-0 (lo)	0x YY71 0000	D(0-31): Counter data 32 LSB	R
0-1: Det-Live-0 (hi)	0x YY71 0004	D(0-7): Counter data 8 MSB	R
ZZ=1			
1-0: Det-Live-1 (lo)	0x YY71 0008	D(0-31): Counter data 32 LSB	R
1-1: Det-Live-1 (hi)	0x YY71 000c	D(0-7): Counter data 8 MSB	R
… and so on			
ZZ = 15			
15-0: Det-Live-15 (lo)	0x YY71 0078	D(0-31): Counter data 32 LSB	R
15-1: Det-Live-15 (hi)	0x YY71 007c	D(0-7): Counter data 8 MSB	R
	0x YY71 0080 – 0x YY71 fffc	Available space for extra pairs of detector-live registers	
For each Trigger XX: XX is in the range 0 to 63 For each XX there is a group of 8 registers Register Address = 0xYY720000 + (XX<<5) + offset			
XX-0: PHYS-XX (lo)	Offset = 0x0	D(0-31): Counter data 32 LSB	R
XX-1: PHYS-XX (hi)	Offset = 0x4	D(0-7): Counter data 8 MSB	R
XX-2: PHYS+CONT-XX (lo)	Offset = 0x8	D(0-31): Counter data 32 LSB	R
XX-3: PHYS+CONT-XX (hi)	Offset = 0xc	D(0-7): Counter data 8 MSB	R
XX-4: PHYS+CONT+LIVE-XX (lo)	Offset = 0x10	D(0-31): Counter data 32 LSB	R
XX-5: PHYS+CONT+LIVE-XX (hi)	Offset = 0x14	D(0-7): Counter data 8 MSB	R
XX-6: PHYS+CONT+LIVE+PS-XX (lo)	Offset = 0x18	D(0-31): Counter data 32 LSB	R
XX-7: PHYS+CONT+LIVE+PS-XX (hi)	Offset = 0x1c	D(0-7): Counter data 8 MSB	R
So, for example…			
XX = 0			
0-0: PHYS-0 (lo)	0x YY72 0000	D(0-31): Counter data 32 LSB	R
0-1: PHYS-0 (hi)	0x YY72 0004	D(0-7): Counter data 8 MSB	R
0-2: PHYS+CONT-0 (lo)	0x YY72 0008	D(0-31): Counter data 32 LSB	R
0-3: PHYS+CONT-0 (hi)	0x YY72 000c	D(0-7): Counter data 8 MSB	R
0-4: PHYS+CONT+LIVE-0 (lo)	0x YY72 0010	D(0-31): Counter data 32 LSB	R
0-5: PHYS+CONT +LIVE-0 (hi)	0x YY72 0014	D(0-7): Counter data 8 MSB	R
0-6: PHYS+CONT +LIVE+PS-0 (lo)	0x YY72 0018	D(0-31): Counter data 32 LSB	R
0-7: PHYS+CONT +LIVE+PS-0 (hi)	0x YY72 001c	D(0-7): Counter data 8 MSB	R
XX = 1			
1-0: PHYS-1 (lo)	0x YY72 0020	D(0-31): Counter data 32 LSB	R
1-1: PHYS-1 (hi)	0x YY72 0024	D(0-7): Counter data 8 MSB	R
1-2: PHYS+CONT-1 (lo)	0x YY72 0028	D(0-31): Counter data 32 LSB	R
1-3: PHYS+CONT-1 (hi)	0x YY72 002c	D(0-7): Counter data 8 MSB	R

1-4: PHYS+CONT +LIVE-1 (lo)	0x YY72 0030	D(0-31): Counter data 32 LSB	R
1-5: PHYS+CONT +LIVE-1 (hi)	0x YY72 0034	D(0-7): Counter data 8 MSB	R
1-6: PHYS+CONT +LIVE+PS-1 (lo)	0x YY72 0038	D(0-31): Counter data 32 LSB	R
1-7: PHYS+CONT +LIVE+PS-1 (hi)	0x YY72 003c	D(0-7): Counter data 8 MSB	R
… and so on			
XX = 63			
63-0: PHYS-63 (lo)	0x YY72 07e0	D(0-31): Counter data 32 LSB	R
63-1: PHYS-63 (hi)	0x YY72 07e4	D(0-7): Counter data 8 MSB	R
63-2: PHYS+CONT-63 (lo)	0x YY72 07e8	D(0-31): Counter data 32 LSB	R
63-3: PHYS+CONT-63 (hi)	0x YY72 07ec	D(0-7): Counter data 8 MSB	R
63-4: PHYS+CONT +LIVE-63 (lo)	0x YY72 07f0	D(0-31): Counter data 32 LSB	R
63-5: PHYS+CONT +LIVE-63 (hi)	0x YY72 07f4	D(0-7): Counter data 8 MSB	R
63-6: PHYS+CONT +LIVE+PS-63 (lo)	0x YY72 07f8	D(0-31): Counter data 32 LSB	R
63-7: PHYS+CONT +LIVE+PS-63 (hi)	0x YY72 07fc	D(0-7): Counter data 8 MSB	R
	0x YY72 0800 – 0x YY7f fffc	Available space for extra registers	

Flash Memory Registers

ID: Name	*Address*	*Functionality (default)*	*Access*
0:Flash block select	0x YYa0 0000	D(0-8): Flash Memory block select Values from 0 to 0x1ff are valid	R/W
1:Flash Reset	0x YYa0 0004	D0: Reset flash memory	W

Input Memory Data

Memory Block	*Starting Address*	*Ending Address*	*Data*
DSM Input Memory 0	0x YY80 0000	0x YY83 fffc	Input Channels 0 and 1
DSM Input Memory 1	0x YY84 0000	0x YY87 fffc	Input Channels 2 and3
DSM Input Memory 2	0x YY88 0000	0x YY8b fffc	Input Channels 4 and 5
DSM Input Memory 3	0x YY8c 0000	0x YY8f fffc	Input Channels 6 and 7
Busy Input Memory	0x YY90 0000	0x YY93 fffc	Bits 0:15 = Internal Busy (1) / Live (0) bits Bits 16:31 = External Busy (0) / Live (1) bits